Andrew Stites

EEE 64 – CpE64 Section 2

Wednesday

Lab 12-13

Samuel Wekanda

Lab Objective/Goal:

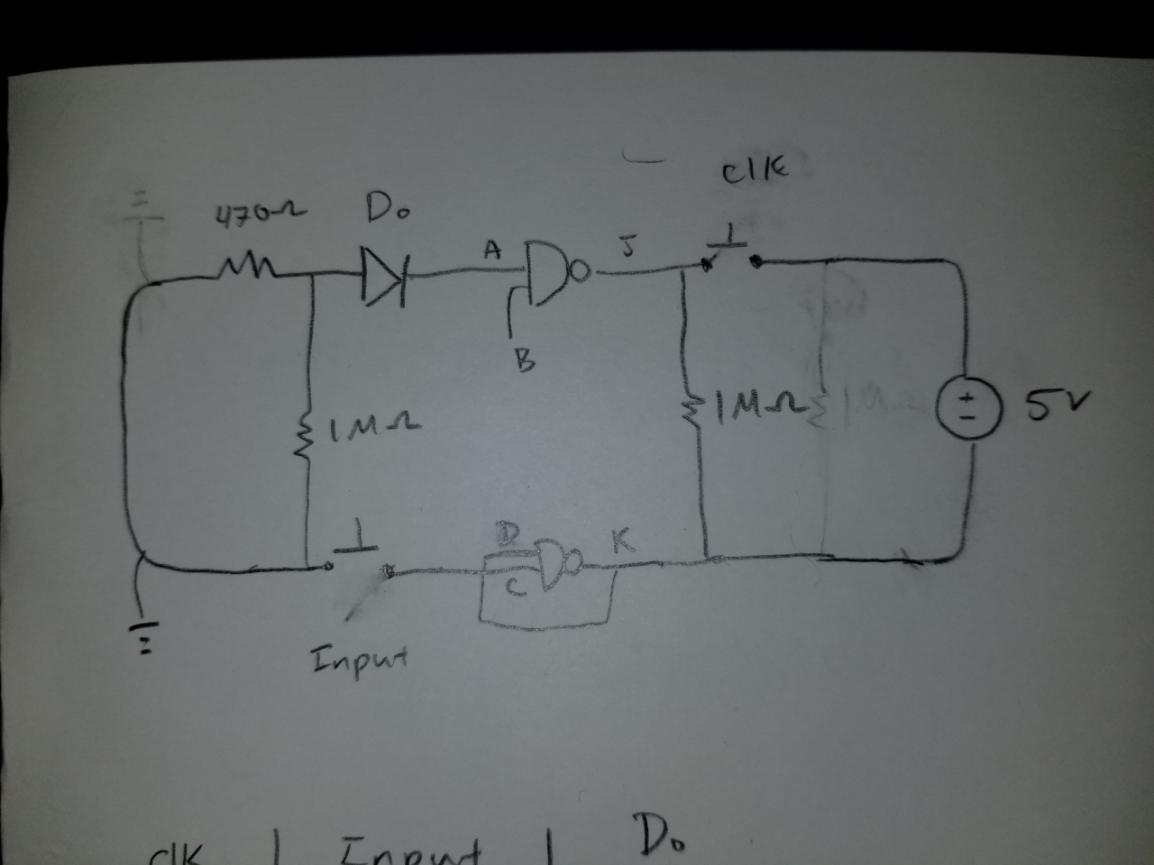
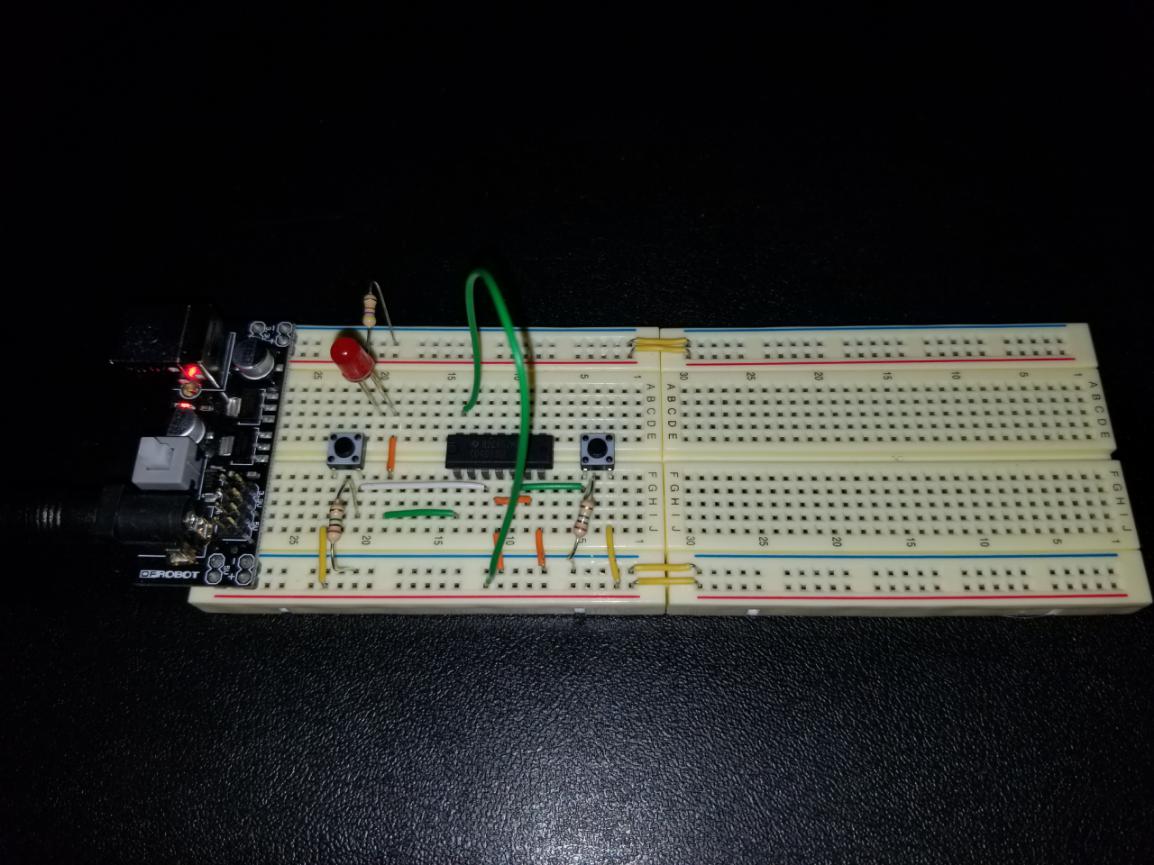
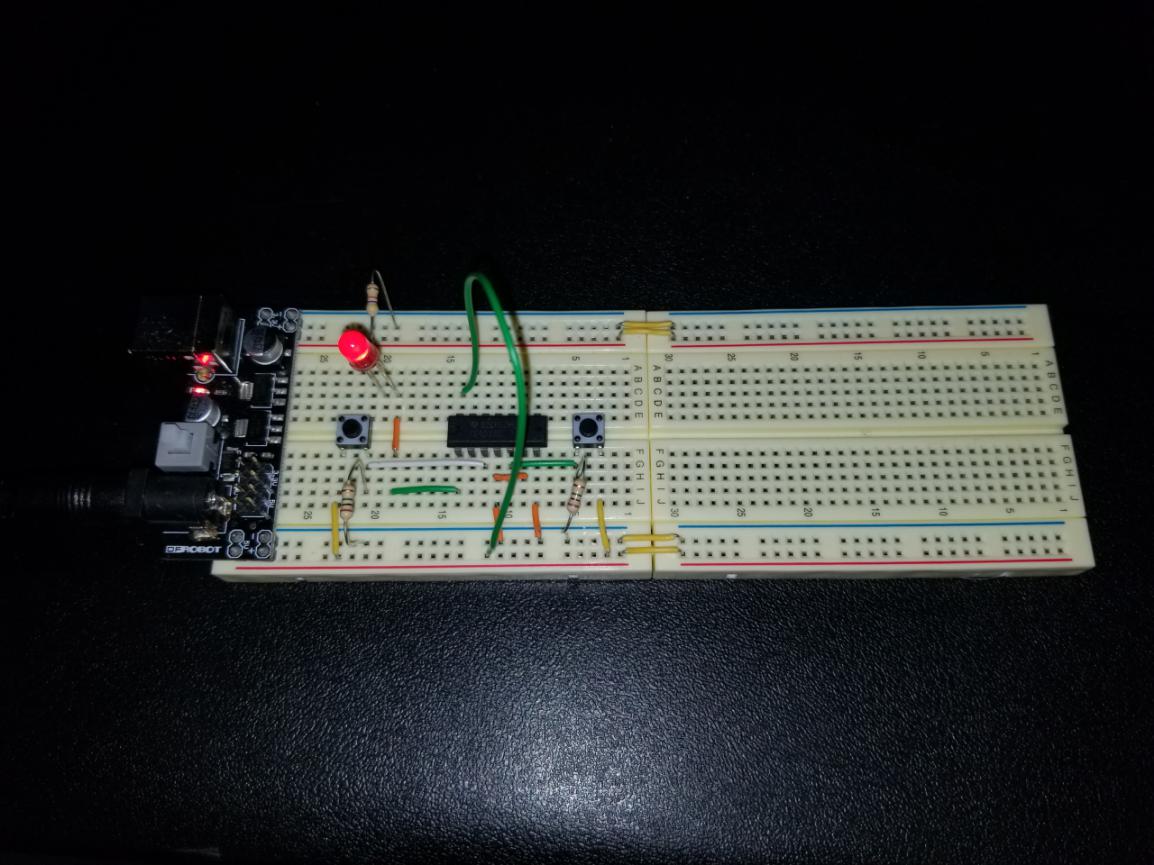
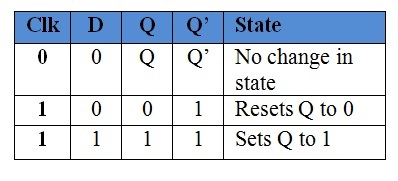
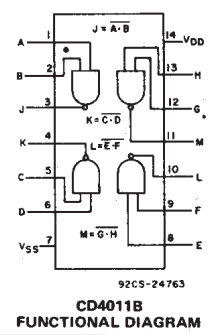
Implement a 1-bit register using a D flip-flop IC on a bread-board. Design a state machine solution for a state diagram using Quartus and Modelsim.

Lab Preparations and Challenges:

I setup my breadboard initially with a red LED connected to ground via a 470 Ohms resistor. The breadboard had two push switches each connected to ground by a 1Mil Ohms resistor. Both push switches were connected to the CD4011BE D-flip flop’s NAND gate inputs. A wire is a connected from the 5V rail to the voltage input for the CD4011BE D-flip flop for proper powering. If “clk” (clock) is Low and the “D”(input) is Low, then it goes into the latched state or the “no change” state. If “clk” (clock) is High and “D” (input) is Low, then the register gets reset to Low or 0. If both “clk” (clock) and “D” (input) are High, then the register gets set to High or 1. Once the breadboard was completed, I made a HDL Verilog file named “StateMachine.v” utilizing case statements to transfer a state machine diagram to ModelSim for WaveForm simulation. A testbench named “StateMachine\_tb().v” was also created to properly compile and run the inputs through the initial file and portray them in green waves denoting correct Mealy and Moore outputs.

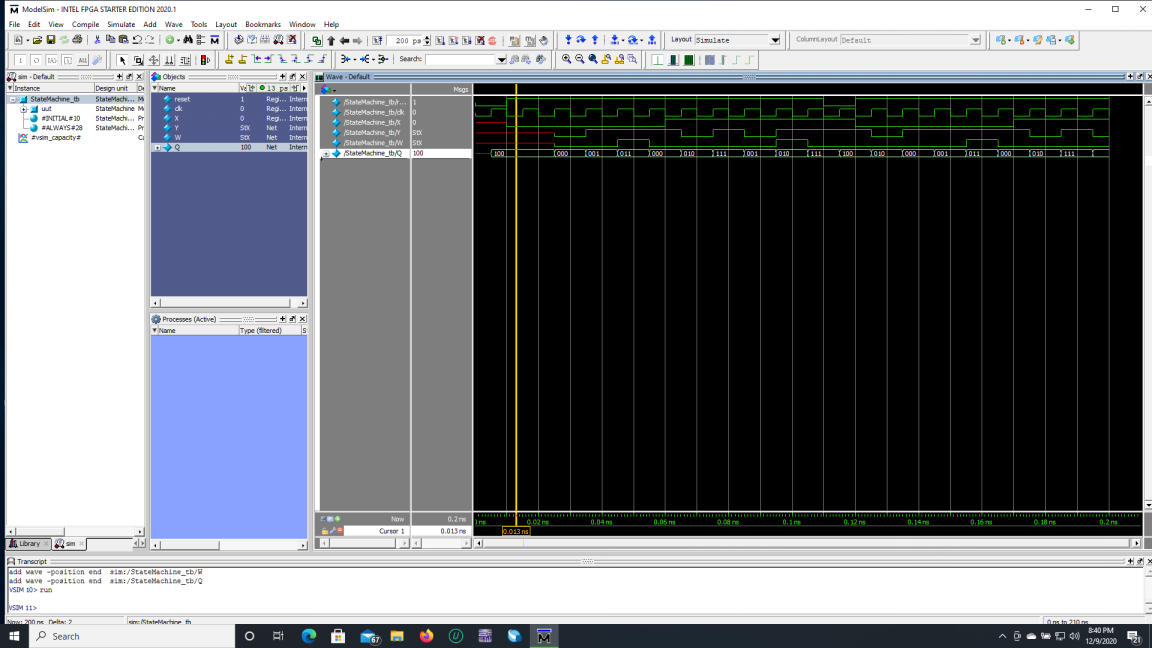
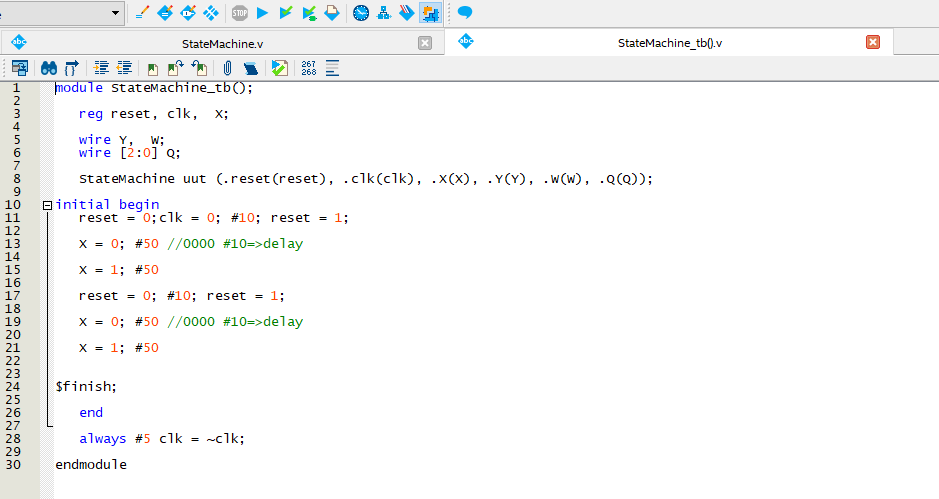
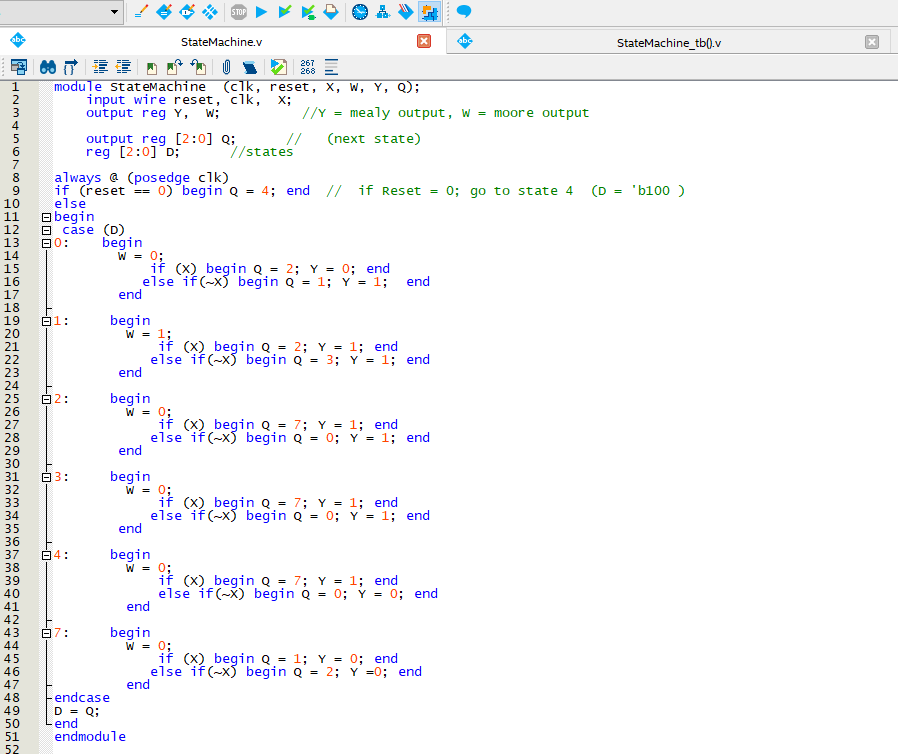
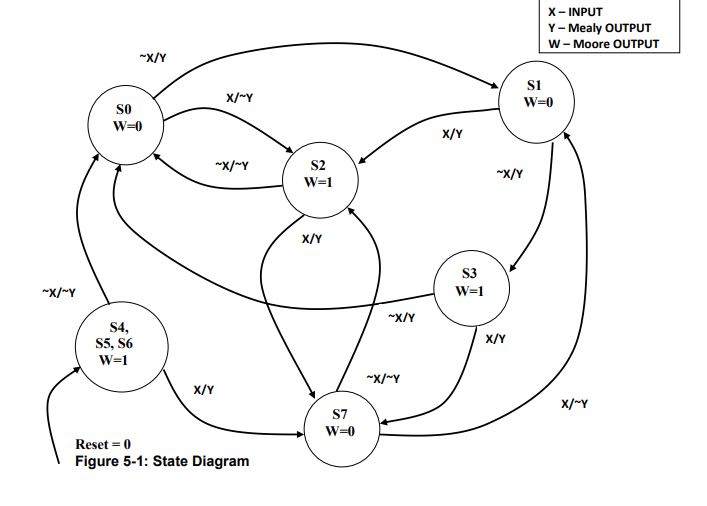
Lab Results:

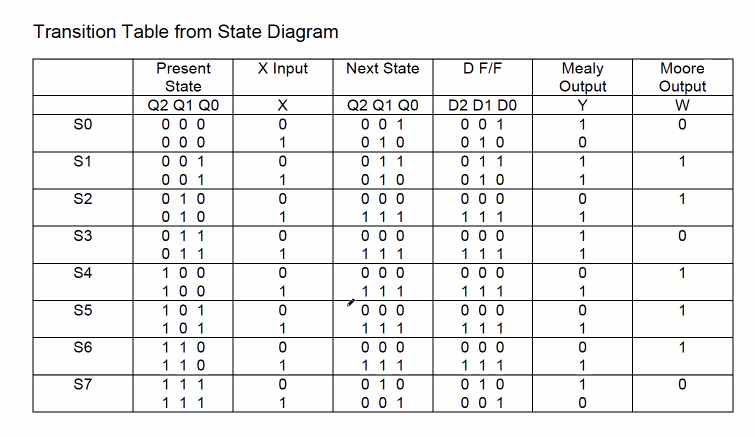
**Circuit Made on BreadBoard:**



The first picture shows the D-flip flop data sheet diagram denoting the inputs and outputs. The second picture shows the truth table regarding the circuit. If “clk” (clock) is Low and the “D”(input) is Low, then it goes into the latched state or the “no change” state. If “clk” (clock) is High and “D” (input) is Low, then the register gets reset to Low or 0. If both “clk” (clock) and “D” (input) are High, then the register gets set to High or 1. The circuit has a 470 Ohms resistor attached to a red LED. There are two push switches, each with a 1Mil Ohms resistor attached, one the “clk”(clock) and the other the “input”. The IC is named CD4011BE and is a D-flip flop with two NAND gates being used on it. The first picture has the “clk”(clock) and “input” set in the High state and the second picture has the “clk”(clock) High and the “input” Low. The picture next is the sketch of the circuit.

**Quartus and ModelSim:**





The first picture illustrates the Mealy and Moore finite state machine diagram with 8 states. All states are accessible with states 4 through 6 being the “reset” state. The next picture shows the intial HDL Verilog code defining states and the pathways they should take to reach another state. The HDL Verilog code utilizes case statements in a loop to properly run through each state depending on the “x”, “clk”, and the “reset” input. The following picture shows the testbench utilized to show portray the logic in the WaveForm editor. Reset was initially set to Low so that the 4th state could be accessed, then set to High so that other states could be accessed. This was while “clk” was oscillating High to Low for the triggered edges to cause a change. The “Transition Table from State Diagram” denotes the inputs for X and the outputs for Moore and Mealy.

Conclusion:

These labs were far more difficult compared to previous. I learned a great amount of Quartus and ModelSim and feel confident regarding future endeavors. Having an extra week to complete both labs made for a more relaxed work environment. I conclude that I did complete both labs, but lab 13 did have one imperfection regarding the reset in the WaveForm editor not matching with the correct state.